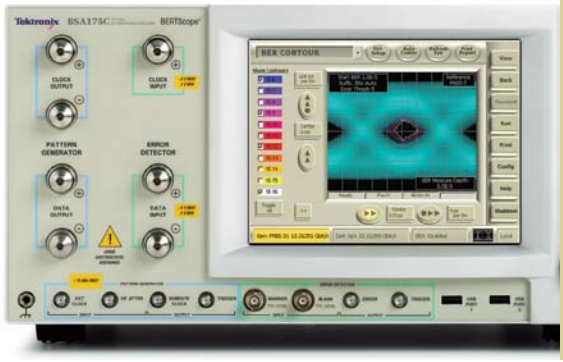
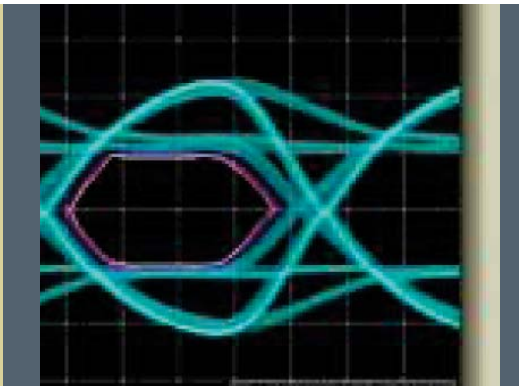




Exploring Power Supply Voltage Sensitivity in an IC with a BERTScope® Bit Error Rate Tester

Application Note

Tektronix®

Introduction

Semiconductor ICs have a specific supply voltage range over which they are guaranteed to operate. While system designers seldom intentionally allow an IC to run outside this range, situations can easily arise where this happens. Often the chip's failure mechanism is unexpected, and not necessarily graceful. In the following example, the prototype chip had its supply voltage deliberately lowered until it started to fail. In this case, the chip was being operated in an Interconnect Built-In Self Test (IBIST) pattern generation mode.

These measurements were taken with a BERTScope BSA175C Series directly from the output of an IC with de-emphasis switched on, giving the characteristic eye shape seen in these measurements. After the appropriate amount of travel through a dispersive medium such as a circuit board, the signal would look like a normal NRZ eye.

As the supply voltage dropped, the first area to fail was internal logic of the pattern generator. This is significant because the high speed interface circuitry in the chip was not affected. The net result is that the chip carried on producing a great looking eye diagram that would fool many kinds of test equipment, but the data being sent was full of errors. Neither eye diagrams nor mask tests alone will pick this up. BER Contours and error-based jitter measurements provided by the BERTScope show the evidence of failure was immediately obvious. This is shown in Figure 1. Note that the eye diagrams look identical.

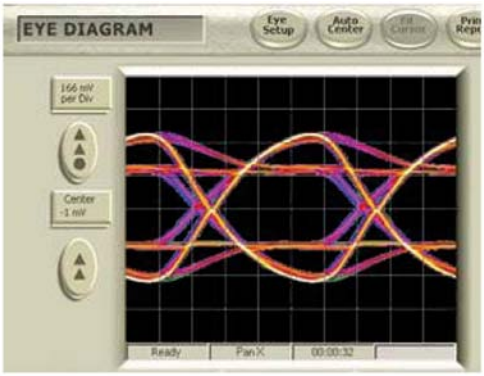
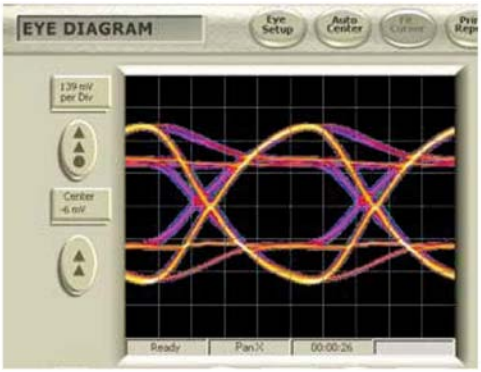
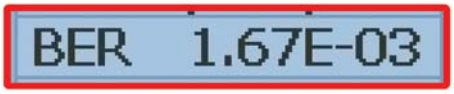
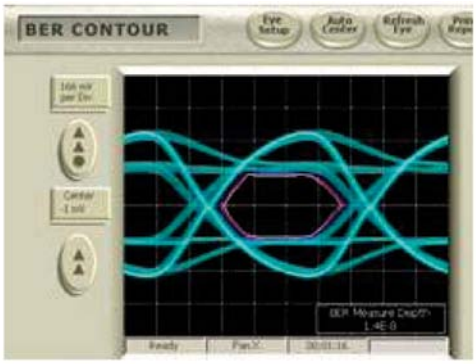
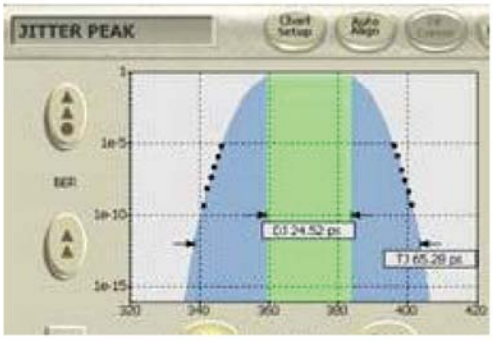
	1.5 V	1.35 V
Eye		
BER		
BER Contour		BER Contour Will Not Run
Jitter Peak		Jitter Peak Will Not Run

Figure 1. Operation at different supply voltages, the left column showing signal integrity measure-ments in the correct operating region. The right column showing measurements following the IBIST pattern generator failing. Note that the eye diagram looks identical in either case, but the BER and related measurements show otherwise.

Summary

We've explored a failure mechanism of a particular IC design. It has exhibited bit errors as the power supply to the chip has dropped below a threshold, but the output waveform has shown no indication of issues arising. This has shown that eye diagrams alone may not be as effective in showing major system issues, and should be coupled with BER-based measurements using the BERTScope BSA Series for deeper insight and problem resolution.

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